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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,218	03/22/2004	James D. Guilford	Intel-023PUS	3297

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Daly, Crowley & Mofford, LLP
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER	
INGBERG, TODD D	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,218	GUILFORD, JAMES D.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/14/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-28* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 28 have been examined.

Drawings

1. The new formal drawings submitted July 1, 2004 have been accepted.

Information Disclosure Statement

2. The Information Disclosure Statement filed July 14, 2005 has been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 14, 17 - 28 rejected under 35 U.S.C. 102(b) as being anticipated by USPN # 5,530,866 **Kob**lenz et al issued June 25, 1996.

Claim 1
Kob anticipates a method of allocating registers in an assembler, comprising: processing assembler code to avoid a register bank allocation error including at least one of a register bank conflict and an insufficient number of physical registers in target hardware; and automatically manipulating instructions to avoid the register bank allocation error. Kob, Abstract – the intent of Kob's invention.

Claim 2
The method according to claim 1, wherein the register bank conflict is associated with instructions in which first and second operands have respective first and second source registers located in a first one of first and second register banks and further including inserting an instruction to assign the first operand to a temporary register. Kob, Col 5, lines 55-63.

Claim 3

The method according to claim 2, wherein the register bank conflict is associated with instructions in which first and second operands have respective first and second source registers located in a first one of first and second register banks and further including inserting an instruction to move the first source register to local memory. Kob, Col 6, lines 40-65.

Claim 4
The method according to claim 1, further including coloring a register graph to detect the register bank conflict. Kob, Col 6, lines 31-35.

Claim 5
The method according to claim 4, further including identifying registers adjacent to each other in the graph having the same color. Kob, Col 13, lines 45-62

Claim 6
The method according to claim 5, further including finding the shortest path having an odd length connecting the registers adjacent to each other having the same color. As per claim 5.

Claim 7
The method according to claim 6, further including sorting a list of edges in the graph associated with path. Kob, Col 14, lines 25-65

Claim 8
The method according to claim 7, further including sorting the list based upon a weight of the edges. Kob, Col 18, lines 12-39.

Claim 9
The method according to claim 8, further including repeating the finding and sorting to find further solutions to color the graph. Kob, Claim 8 and Col 13, lines 15-45.

Claim 10
The method according to claim 1, further including manipulating instructions to spill one or more registers associated with the assembler code to alternative memory in the target hardware. Kob, Col 17, lines 1-15.

Claim 11
The method according to claim 10, further including mapping virtual registers to physical registers and spilling a sufficient number of physical registers to enable mapping between the virtual registers and the physical registers in the target hardware. As per claim 1 – intent of the invention.

Claim 12
The method according to claim 10, wherein the non-register memory includes one or more of local memory Kob, Col 6, lines 57-65, SRAM memory and DRAM memory.

Claim 13
The method according to claim 10, further including identifying registers that should not be spilled. Kob, Col 17, lines 51-60 – not part of the loop.

Claim 14
The method according to claim 10, further including determining first and second banks of abstract physical registers for target hardware having alternative memory with a single read port. As per claim 1.

Claim 17
An article, comprising: a storage medium having stored thereon instructions that when executed by a machine result in the following: processing assembler code to avoid a register bank allocation error including at least one of a register bank conflict and insufficient number of physical registers in target hardware; and automatically manipulating instructions to avoid the register bank allocation error. See the rejection for claim 1.

Claim 18
The article according to claim 17, wherein the register bank conflict is generated by instructions in which first and second operands have respective first and second source registers located in a first one of first and second register banks and further including inserting instructions to assign the first operand to a temporary register and/or local memory. See the rejection for claim 2.

Claim 19
The article according to claim 18, further including stored instructions to color a register graph to detect the register bank conflict. See the rejection for claim 4.

Claim 20
The article according to claim 19, further including stored instructions to spill one or more virtual registers associated with the assembler code. See the rejection for claim 10.

Claim 21
The article according to claim 20, further including stored instruction to spill a sufficient number of registers so that non-spilled ones of the registers can be mapped to physical registers in the target hardware. See the rejection for claim 11.

Claim 22
The article according to claim 21, further including stored instructions to identify registers that should not be spilled. See the rejection for claim 13.

Claim 23
A development/debugger system, comprising: an assembler to generate microcode that is executable in a processing element by processing assembler code to avoid a register bank allocation error including at least one of a register bank conflict and insufficient number of

physical registers in target hardware; and automatically manipulating instructions to avoid the register bank allocation error. See the rejection for claim 1.

Claim 24
The system according to claim 23, wherein the register bank conflict is generated by instructions in which first and second operands have respective first and second source registers located in a first one of first and second register banks and further including inserting instructions to assign the first operand to a temporary register and/or local memory. See the rejection for claim 2.

Claim 25
The system according to claim 24, wherein the register bank conflict is generated by the insufficient number of physical registers and wherein manipulating the instructions includes spilling one or more of the physical registers to alternative memory. See the rejection for claim 10 and claim 11.

Claim 26
A network forwarding device, comprising: at least one line card to forward data to ports of a switching fabric; the at least one line card including a network processor having multi-threaded microengines configured to execute microcode, wherein the microcode comprises a microcode developed using an assembler that processed assembler code to avoid a register bank allocation error including at least one of a register bank conflict and insufficient number of physical registers in target hardware; and automatically manipulated instructions to avoid the register bank allocation error. See the rejection for claim 1.

Claim 27
The device according to claim 26, wherein the register bank conflict was generated by instructions in which first and second operands have respective first and second source registers located in a first one of first and second register banks and further including inserting an instruction to assign the first operand to a temporary register and/or local memory.
28. The device according to claim 27, wherein the register bank conflict was generated by the insufficient number of physical registers and wherein the inserted instructions include spilling one or more of the physical registers to alternative memory. See the rejection for claim 2.

Claim 28
The device according to claim 27, wherein the register bank conflict was generated by the insufficient number of physical registers and wherein the inserted instructions include spilling one or more of the physical registers to alternative memory. See the rejection for claim 10.

Allowable Subject Matter

5. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Correspondence Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Todd Ingberg
Primary Examiner
Art Unit 2193

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